

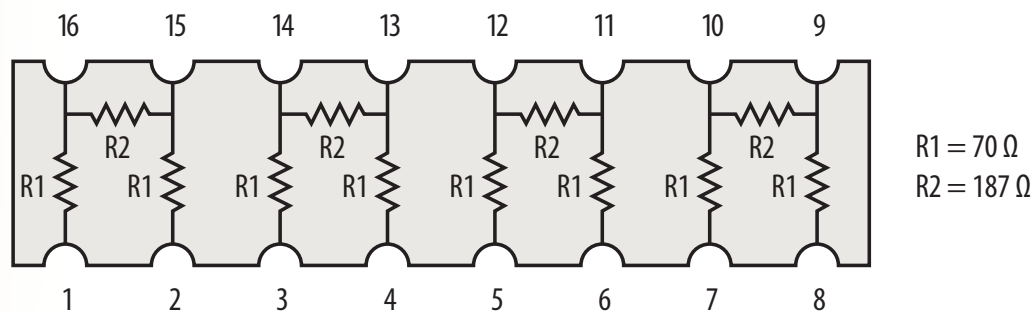
CAT16-PC5F12LF

The continuing growth in communications and the need for higher bandwidths together with reduced power consumption has made LVDS a very popular choice with board designers. LVDS is a differential signaling standard which uses two wires with opposite current/voltage swings and is less susceptible to EMI and noise than single ended methods. This reduction in interference means that lower voltage swings and higher switching speeds (>400 Mbps) are possible as well.

The Virtex series of FPGAs from Xilinx support the LVDS standard. Xilinx recommends the use of terminating resistors for the driver and receiver FPGAs (source termination and load termination).

The Virtex-4 user guide recommends two series resistors (RS) of 70 Ω and one parallel resistor (Rdiv) of 187 Ω for matching the source impedance and attenuating any reflections from the load. The Bourns® CAT16-PC5F12LF resistor array contains four groups of the recommended resistors to support the Virtex-4 FPGA operation.

The internal schematic is shown below:



Bourns offers seven different resistor array types designed for matching the source impedance or load impedance of the Virtex Family of FPGAs. The link below will access the datasheets for these devices.

<http://www.bourns.com/components.aspx?cmsphid=7631383|7163299|6030957>

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